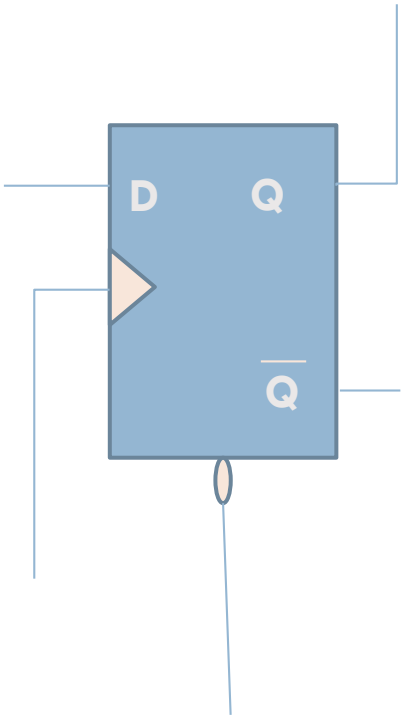
REGISTERS

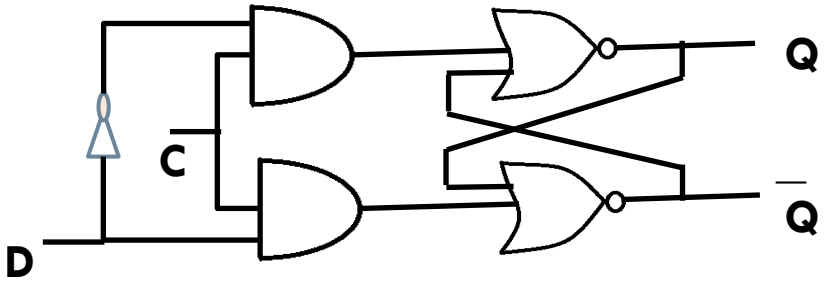
Compiled By: Afaq Alam Khan

Register

- A register is a group of binary storage cells suitable for holding binary information. A group of flip-flops constitutes a register, since each flip-flop is a binary cell capable of storing one bit of information.
- An n-bit register has a group of n flip-flops and is capable of storing any binary information containing n bits.

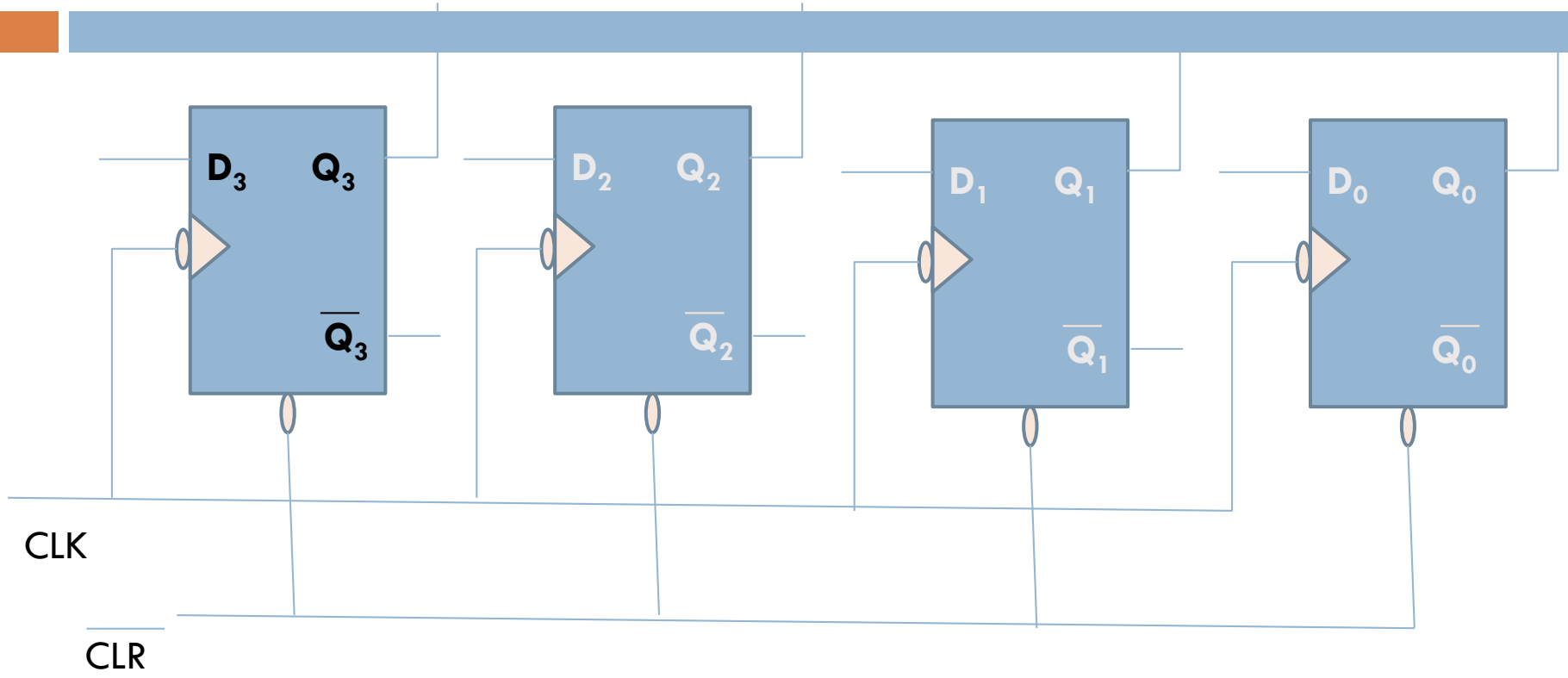
Recap – D Flipflop





D	Q(t+1)	
0	0	Clear
1	1	Set

Example – 4 bit Register



Data inputs are given at the D inputs of the flipflops.

The four bit data is transferred to the outputs at the **falling edge** of the clock pluse

Example of PIPO

Shift Register

- The Shift Register is another type of sequential logic circuit that can be used for the storage or the transfer of binary data

- A *shift register* basically consists of several single bit "D-Type Data Latches", one for each data bit, either a logic "0" or a "1", connected together in a serial arrangement so that the output from one data latch becomes the input of the next latch and so on.

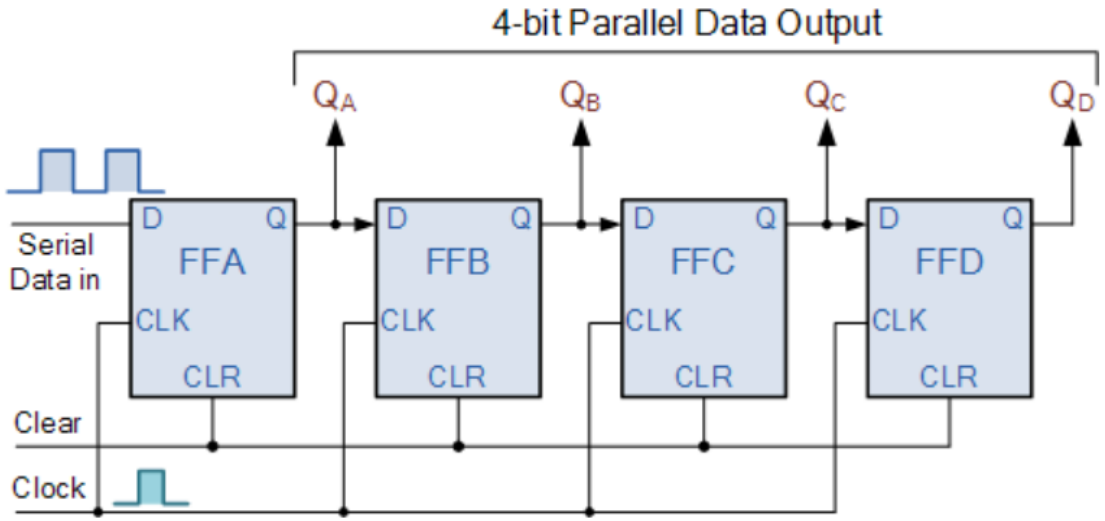
- Data bits may be fed in or out of a shift register serially, that is one after the other from either the left or the right direction, or all together at the same time in a parallel configuration.
- The individual data latches that make up a single shift register are all driven by a common clock (Clk) signal making them synchronous devices.

Shift Registers

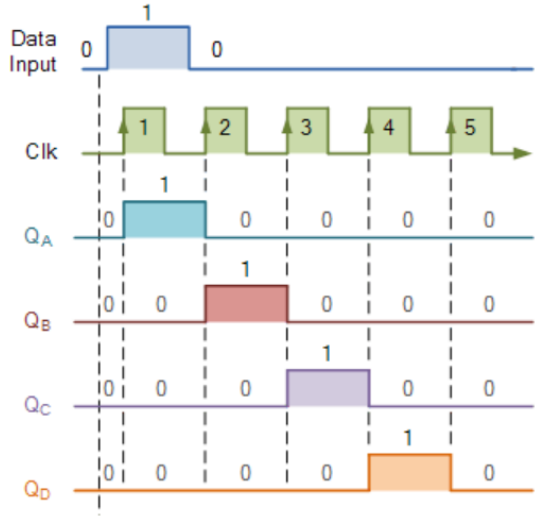
- Generally, shift registers operate in one of four different modes with the basic movement of data through a shift register being:
  - **Serial-in to Parallel-out (SIPO)** - the register is loaded with serial data, one bit at a time, with the stored data being available at the output in parallel form.
  - **Serial-in to Serial-out (SISO)** - the data is shifted serially "IN" and "OUT" of the register, one bit at a time in either a left or right direction under clock control.
  - **Parallel-in to Serial-out (PISO)** - the parallel data is loaded into the register simultaneously and is shifted out of the register serially one bit at a time under clock control.
  - **Parallel-in to Parallel-out (PIPO)** - the parallel data is loaded simultaneously into the register, and transferred together to their respective outputs by the same clock pulse.

4-bit Serial-in to Parallel-out Shift Register (SIPO)

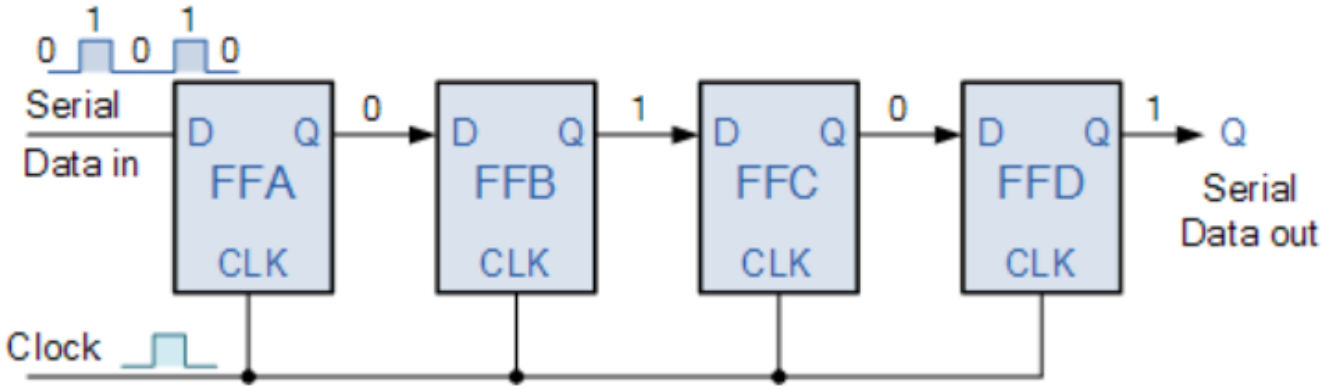
Commonly available SIPO IC's include the standard 8-bit 74LS164 or the 74LS594.



Clock Pulse No	QA	QB	QC	QD
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	0	0	1	0
4	0	0	0	1
5	0	0	0	0



4-bit Serial-in to Serial-out Shift Register (SISO)



Commonly available IC's include the 74HC595 8-bit Serial-in to Serial-out Shift Register

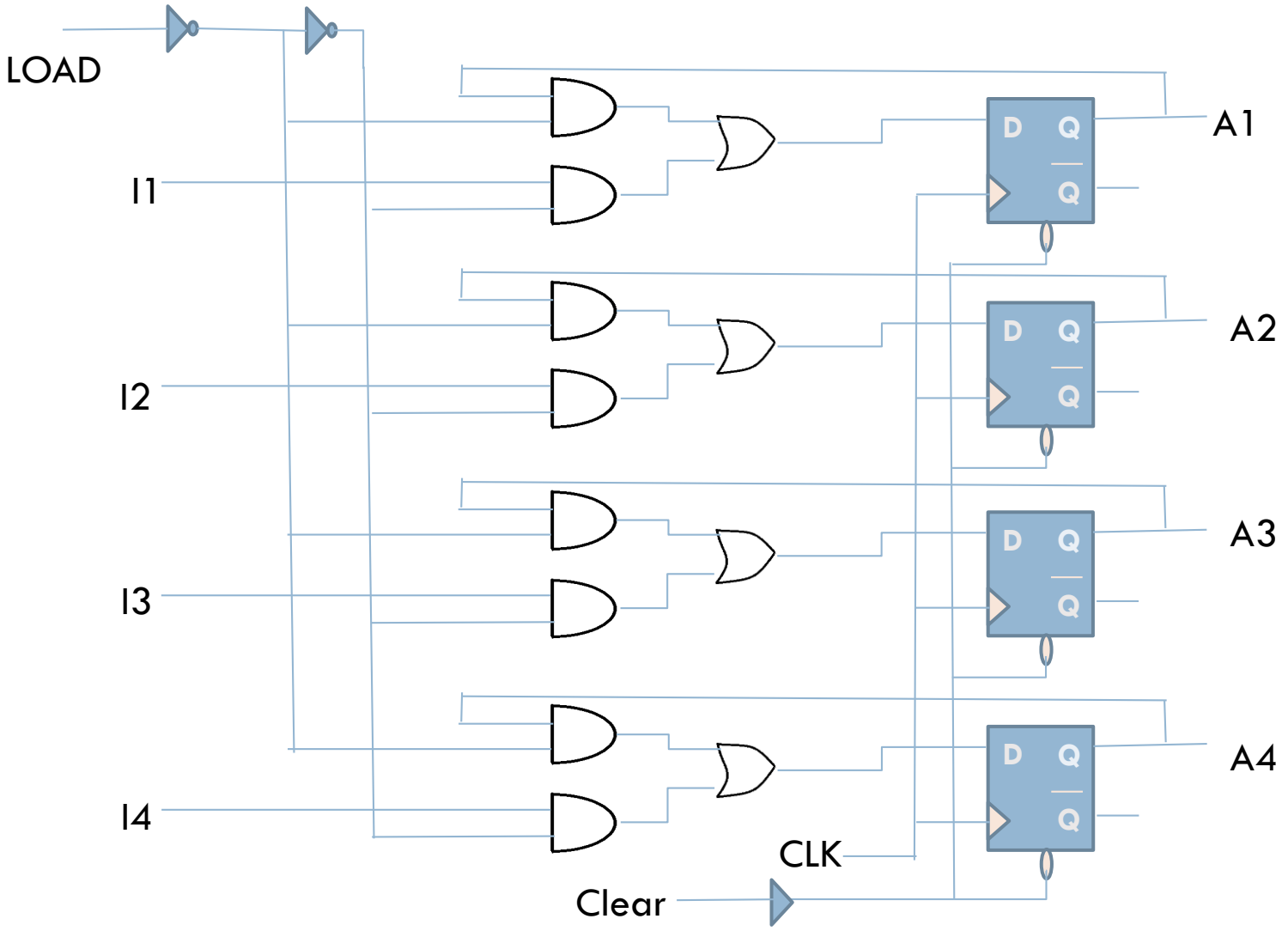
4-bit Parallel-in to Serial-out Shift Register (PISO)

- Self Study

Parallel-in to Parallel-out Shift Register (PIPO)

- Transfer of new information into register is referred to as loading the register
- If all the bits of the register are loaded simultaneously with a single clock pulse, we say that the loading is done in parallel.

4 bit Parallel-in to Parallel-out Shift Register (PIPO) with Load line



4 bit Parallel-in to Parallel-out Shift Register (PIPO)

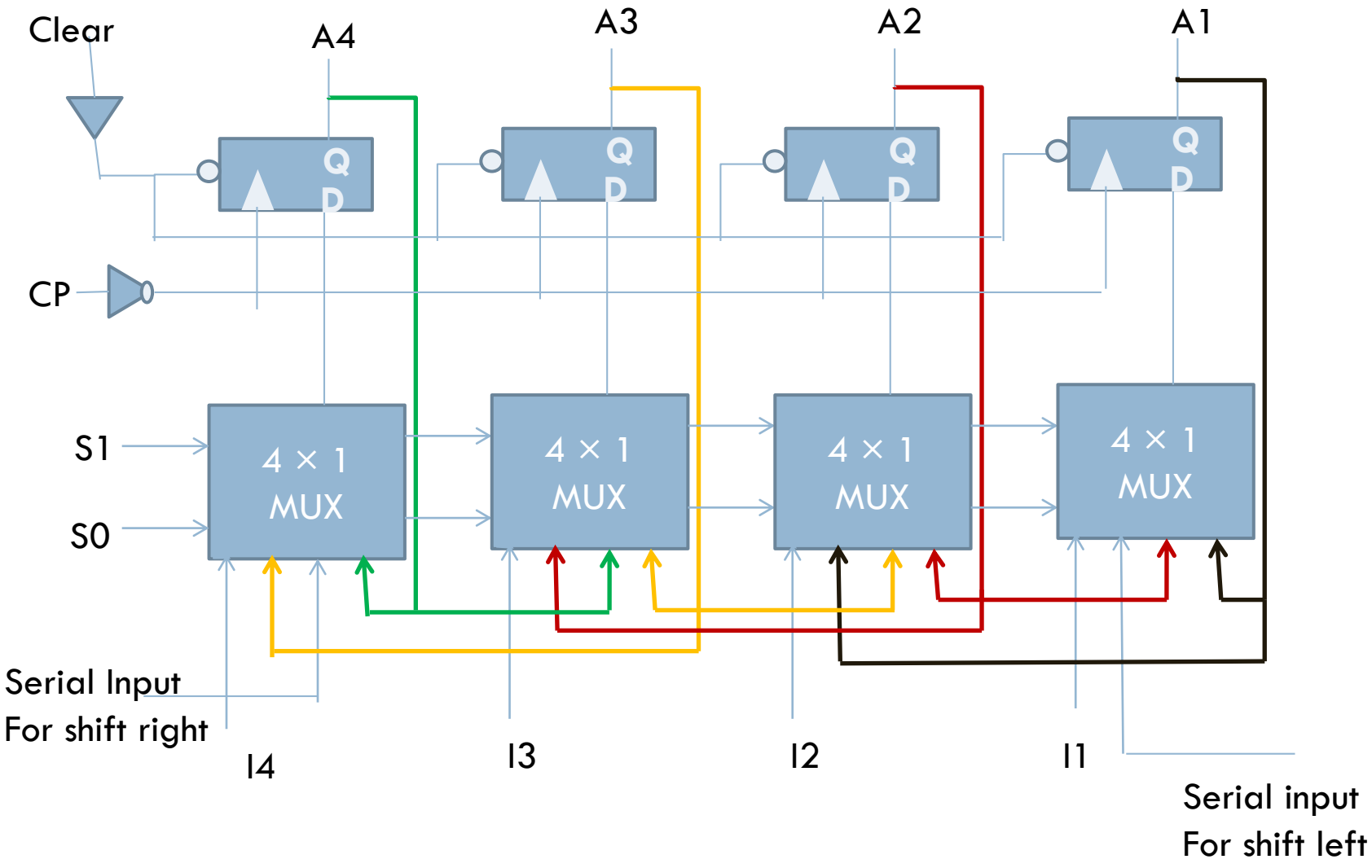
- The **CP input** of the register receives continious synchronized pulses which are applied to all flip flops.
- The **clear input** goes to a special terminal in each flipflop through a buffer gate. When this input goes to 0 , the FF is cleared asynchronously. This input must be maintained at 1 during normal operation.
- When the **load input** is 1, the I inputs are transferred into the register on the next clock pulse.
- When the load input is 0, the circuit inputs are inhibited and the D flip-flops are reloaded with their present value, thus maintaining the content of register.
- D flip flop does not have a no-change input condition. With each clock pulse, the D input determines the next state of the output. To leave the output unchanged, it is necessary to make the D input equal to the present Q output of each flipflop

Bidirectional shift register with parallel Load

- A register capable of shifting both right and left is called bidirectional shift register.

- A bidirectional shift register with a parallel load is a general purpose register capable of performing three operations:
  - Shift right
  - Shift left
  - Parallel load

Bidirectional shift register with parallel Load



Bidirectional shift register with parallel Load

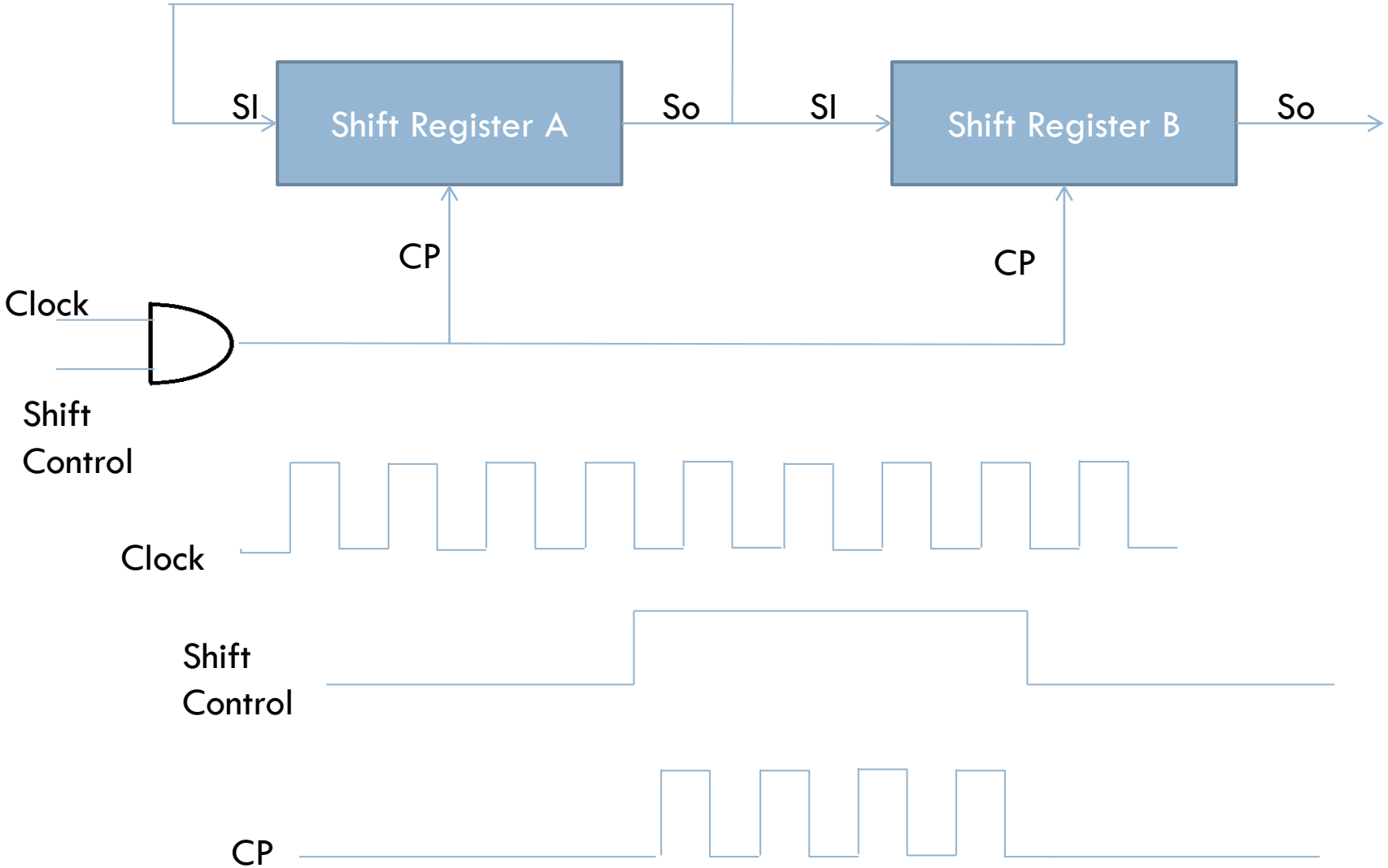
- Mode Control
  - S1 S0 = 00 -> No change
  - S1 S0 = 01 -> Shift right
  - S1 S0 = 10 -> Shift left
  - S1 S0 = 11 -> parallel load

Serial Transfer using shift registers

- A digital system is said to operate in a serial mode when information is transferred and manipulated one bit at a time.

- The content of one register is transferred to another by shifting the bits from one register to the other.

Serial Transfer using shift registers



Serial Transfer

- The contents of A is transferred into B while the contents of A remain unchanged.

- Time interval between clock pulses is called **bit time,** and the time required to shift the entire contents of a shift register is called the **word time.**

Reference

- M. Morris Mano, “Digital Logic and Computer Design”, Pearson
- https://www.electronics-tutorials.ws/sequential/seq_5.html