COUNTERS

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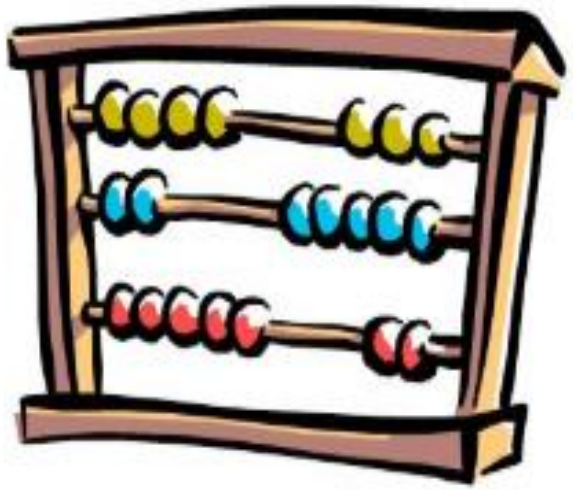


Counters

- Counters are sequential logic circuits that proceed through a well defined sequence of states after application of clock pulses.
- Special type of registers with a capability of counting with the application of clock pulse
- Counters are used for a counting pulses
- Counters are constructed using Flipflops and logic gates
- Counters are classified into two categories
  - Ripple (or Asynchronous) Counters
  - Synchronous Counters

Ripple Counters (Asynchronous Counters)

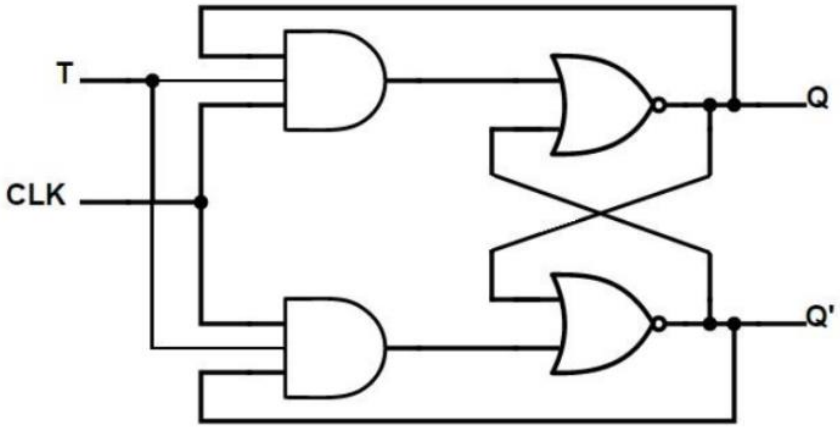
- Clock connected to the flip-flop clock input on the LSB bit flip-flop
- For all other bits, a flip-flop output is connected to the clock input, thus circuit is not truly synchronous!
- Output change is delayed more for each bit toward the MSB.
- An n-bit **Asynchronous counter** can have 2^n possible counting states e.g. MOD-8 for a 3-bit counter have (0-7) states

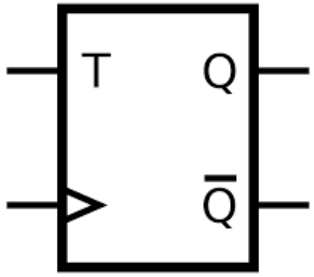
000
001
010
011
100
101
110
111

- But it is also possible to use the basic asynchronous counter configuration to construct special counters with counting states less than their maximum output number.
- This is achieved by forcing the counter to reset itself to zero at a pre-determined value producing a type of asynchronous counter that has truncated sequences.
- Then an n-bit counter that counts up to its maximum modulus (2^n) is called a **full sequence counter** and a n-bit counter whose modulus is less than the maximum possible is called a **truncated counter**.

Recap

- **T Flip flop**

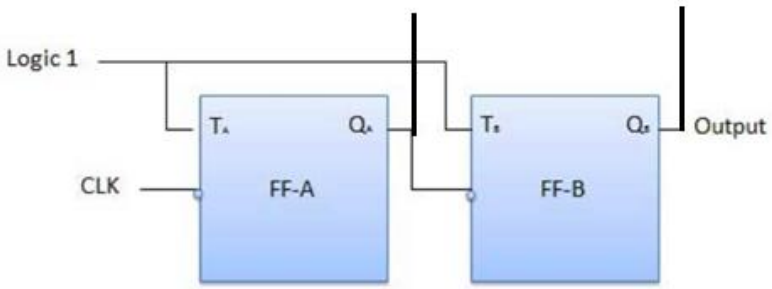




Clk	T	Q(t+1)	
0	X	Q(t)	No change
0→1	0	Q(t)	No change
1→1	1	Q'(t)	Complement

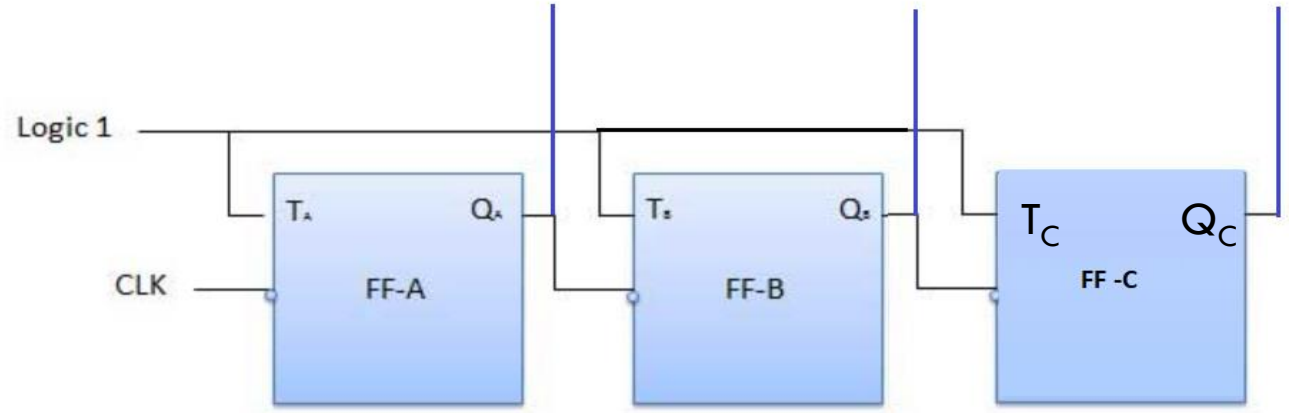
2-bit Ripple Up Counter (MOD-4)

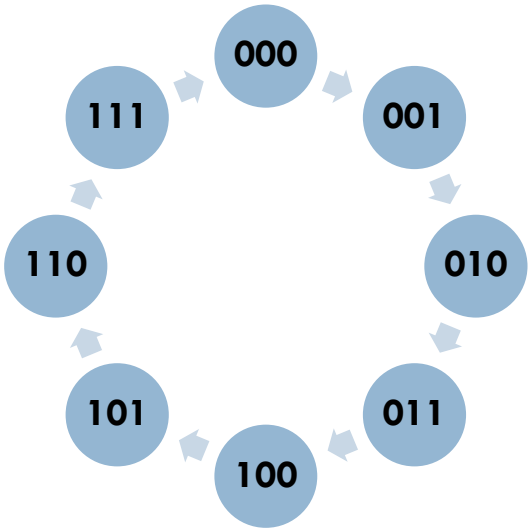
- The toggle (T) flip-flop are being used. But we can use the JK flip-flop also with J and K connected permanently to logic 1. External clock is applied to the clock input of flip-flop A and Q_A output is applied to the clock input of the next flip-flop i.e. FF-B.



Clock	Counter output		State number	Deciimal Counter output
	Q_B	Q_A		
Initially	0	0	—	0
1st	0	1	1	1
2nd	1	0	2	2
3rd	1	1	3	3
4th	0	0	4	0

3-bit Ripple Up Counter (MOD-8)



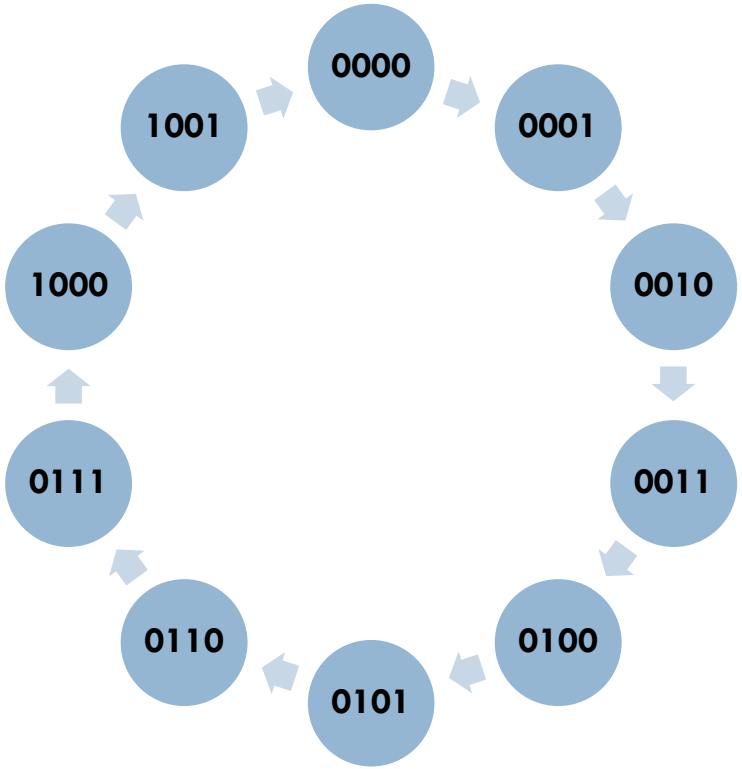


Exercise 1

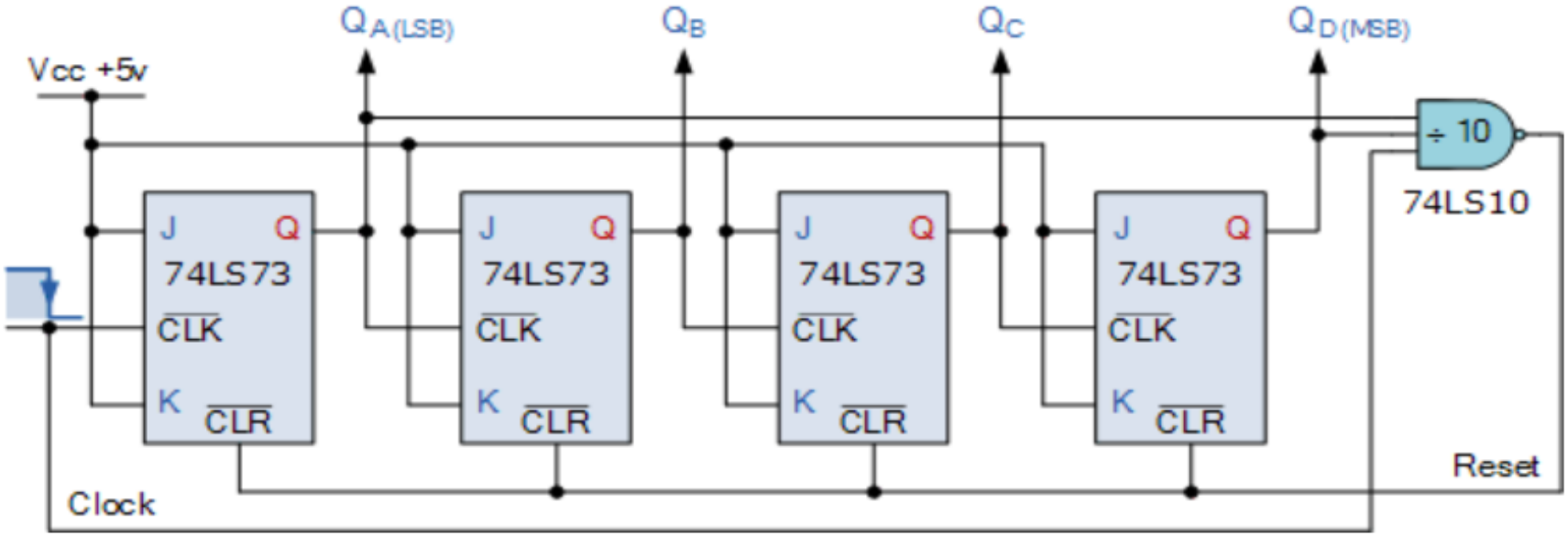
- A) Design and explain MOD-16 Asynchronous UP counter.
- B) Design and explain MOD-16 Asynchronous UP counter using D Flipflops

Ripple Counter (Truncated) Decade Counter

- **Decade Counter (MOD-10)**
- Also called BCD counter
- For a counter to count from 0000 to 1001, four flip flops are required. But we need to mechanism to restrict the count to 1001 and thereafter reset the counter to 0000 again otherwise our counter (with 4 flip flops) will continue to 1111 making it MOD-16 counter instead of MOD-10.



Decade Counter



https://www.electronics-tutorials.ws/counter/count_2.html

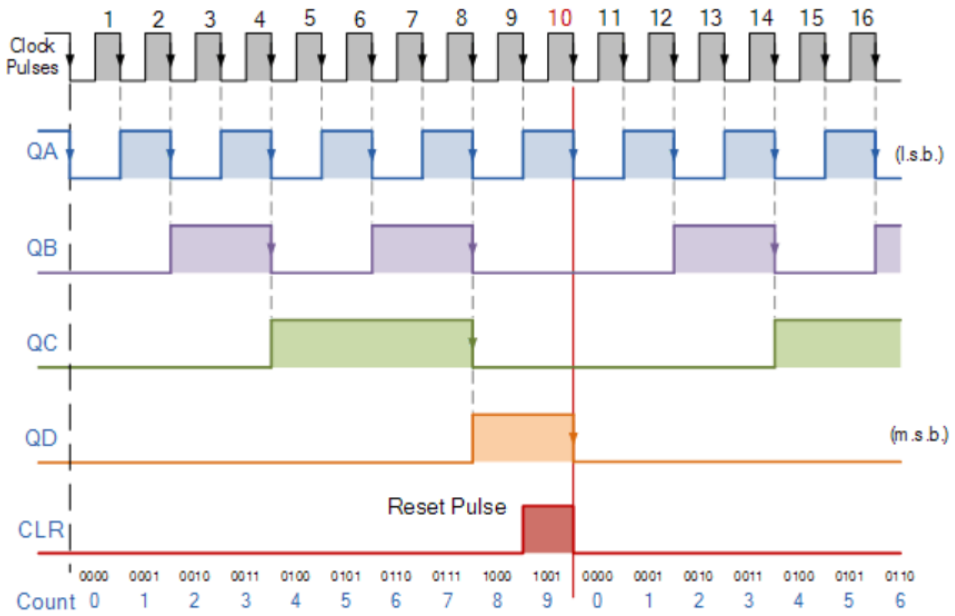
- This type of asynchronous counter counts upwards on each trailing edge of the input clock signal starting from 0000 until it reaches an output 1001 (decimal 9). Both outputs QA and QD are now equal to logic "1". On the application of the next clock pulse, the output from the 74LS10 NAND gate changes state from logic "1" to a logic "0" level.

Decade Counter

- As the output of the NAND gate is connected to the CLEAR (CLR) inputs of all the 74LS73 J-K Flip-flops, this signal causes all of the Q outputs to be reset back to binary 0000 on the count of 10.

- As outputs QA and QD are now both equal to logic “0” as the flip-flop’s have just been reset, the output of the NAND gate returns back to a logic level “1” and the counter restarts again from 0000. We now have a decade or Modulo-10 up-counter.

Decade Counter

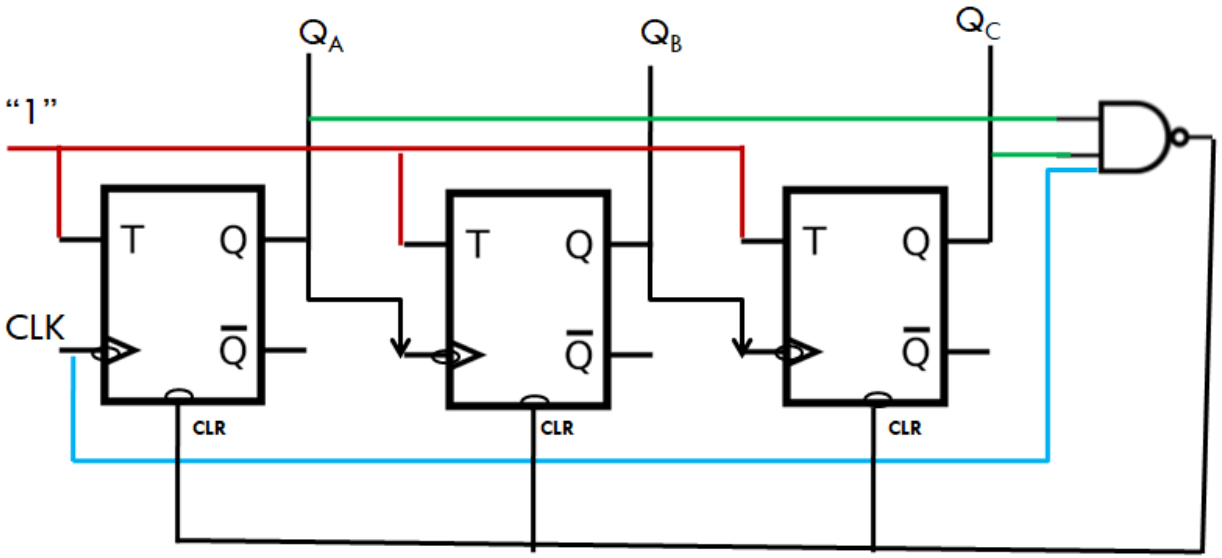


Clock Count	Output bit Pattern				Decimal Value
	QD	QC	QB	QA	
1	0	0	0	0	0
2	0	0	0	1	1
3	0	0	1	0	2
4	0	0	1	1	3
5	0	1	0	0	4
6	0	1	0	1	5
7	0	1	1	0	6
8	0	1	1	1	7
9	1	0	0	0	8
10	1	0	0	1	9
11	Counter Resets its Outputs back to Zero				

- By using the same idea of truncating counter output sequences, the above circuit could easily be adapted to other counting cycles be simply changing the connections to the inputs of the NAND gate or by using other logic gate combinations.

MOD-6 Asynchronous Up Counter

- MOD 6 asynchronous counter will require 3 flip flops and will count from 000 to 101.

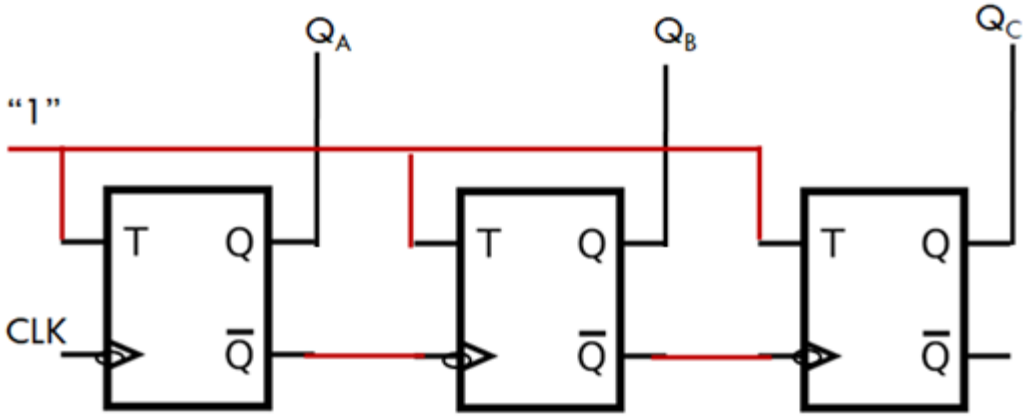


Q_C	Q_B	Q_A
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1

- Once the Counter reaches 101, next positive edge of the clock will make all three inputs of NAND gate as 1 and will set its output to 0 which is connected to CLR of all the flipflops thereby forcing all the flipflops to reset to 0. With the result counter is reset to 000.

Asynchronous Down Counter

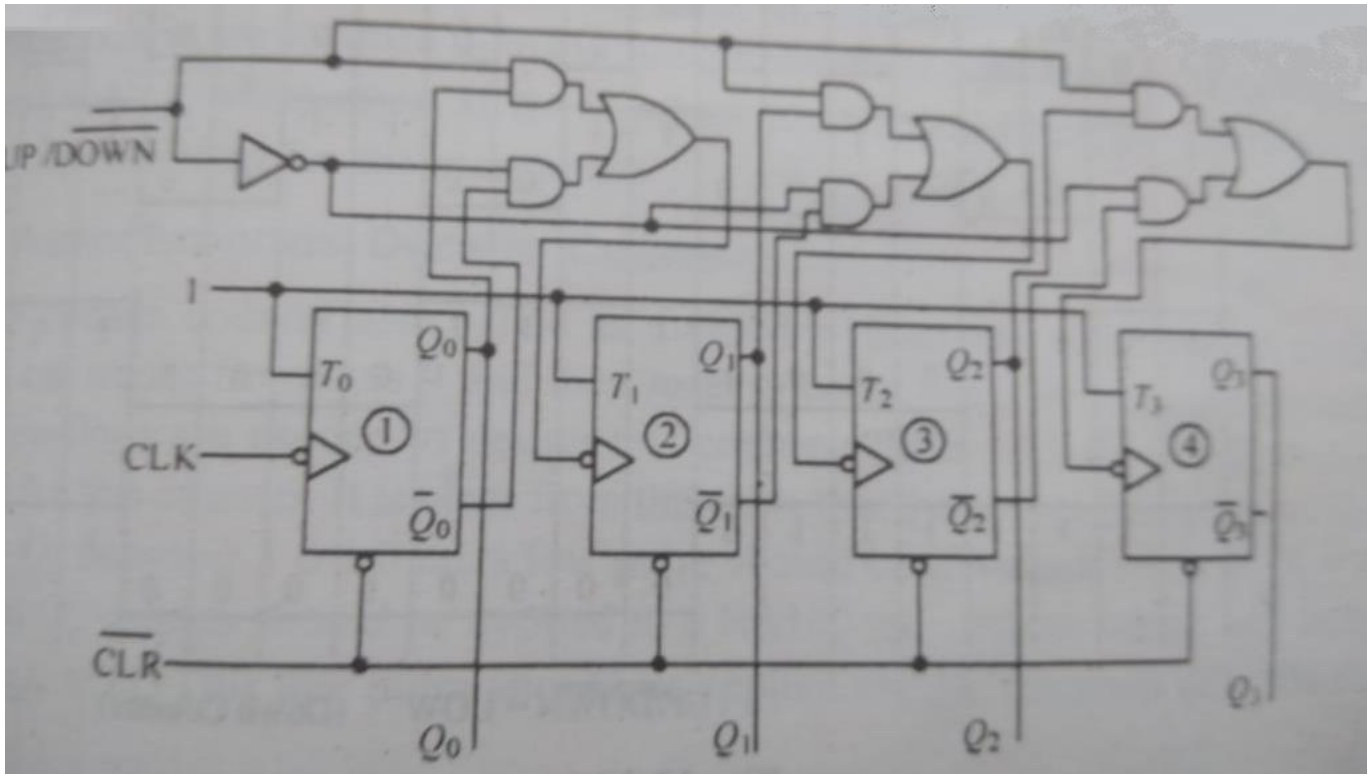
- MOD 8 Down Counter



Q_C	Q_B	Q_A
1	1	1
1	1	0
1	0	1
1	0	0
0	1	1
0	1	0
0	0	1
0	0	0

Asynchronous UP-Down Counter

- MOD-16 UP-DOWN counter

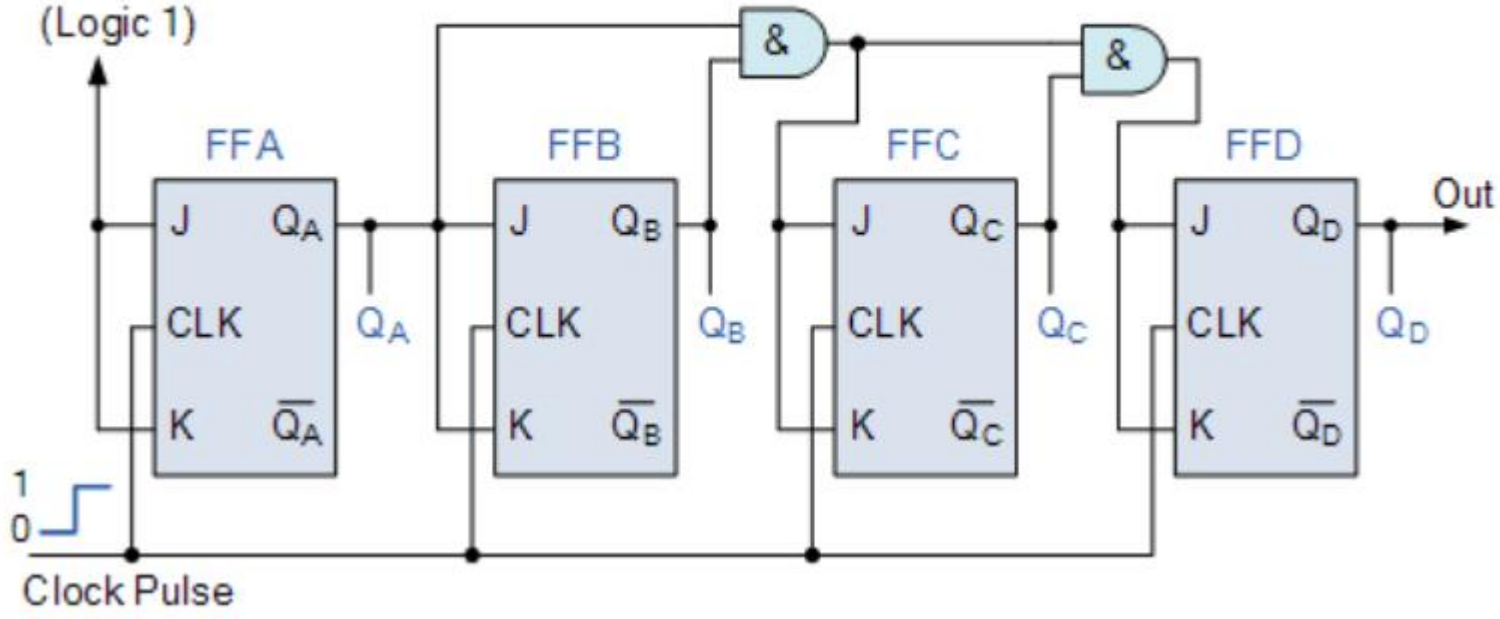


UP/Down = 1 → UP Counter
UP/Down = 0 → Down Counter

Synchronous Counters

- In **Synchronous Counter,** the external clock signal is connected to the clock input of EVERY individual flip-flop within the counter so that all of the flip-flops are clocked together simultaneously (in parallel) at the same time giving a fixed time relationship. In other words, changes in the output occur in "synchronisation" with the clock signal.
- The result of this synchronisation is that all the individual output bits changing state at exactly the same time in response to the common clock signal with no ripple effect and therefore, no propagation delay.

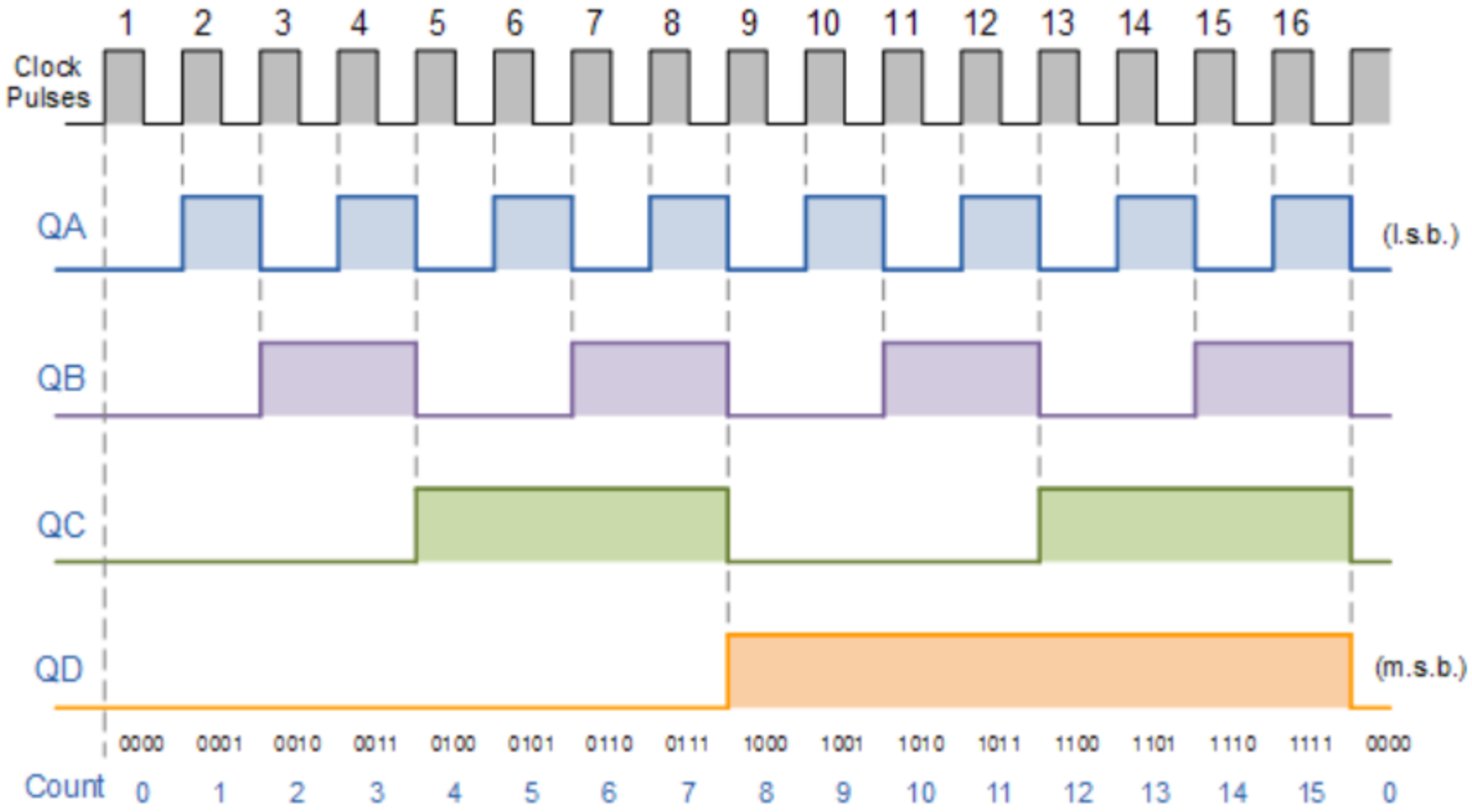
Binary 4-bit Synchronous Up Counter



- External clock pulses (pulses to be counted) are fed directly to each of the **J-K flip-flops** in the counter chain and that both the J and K inputs are all tied together in toggle mode (High), but only in the first flip-flop, FFA (LSB) allowing the flip-flop to toggle on every clock pulse. Then the synchronous counter follows a predetermined sequence of states in response to the common clock signal, advancing one state for each pulse.
- The J and K inputs of flip-flop FFB are connected directly to the output Q_A of flip-flop FFA, but the J and K inputs of flip-flops FFC and FFD are driven from separate AND gates which are also supplied with signals from the input and output of the previous stage. These additional AND gates generate the required logic for the JK inputs of the next stage.

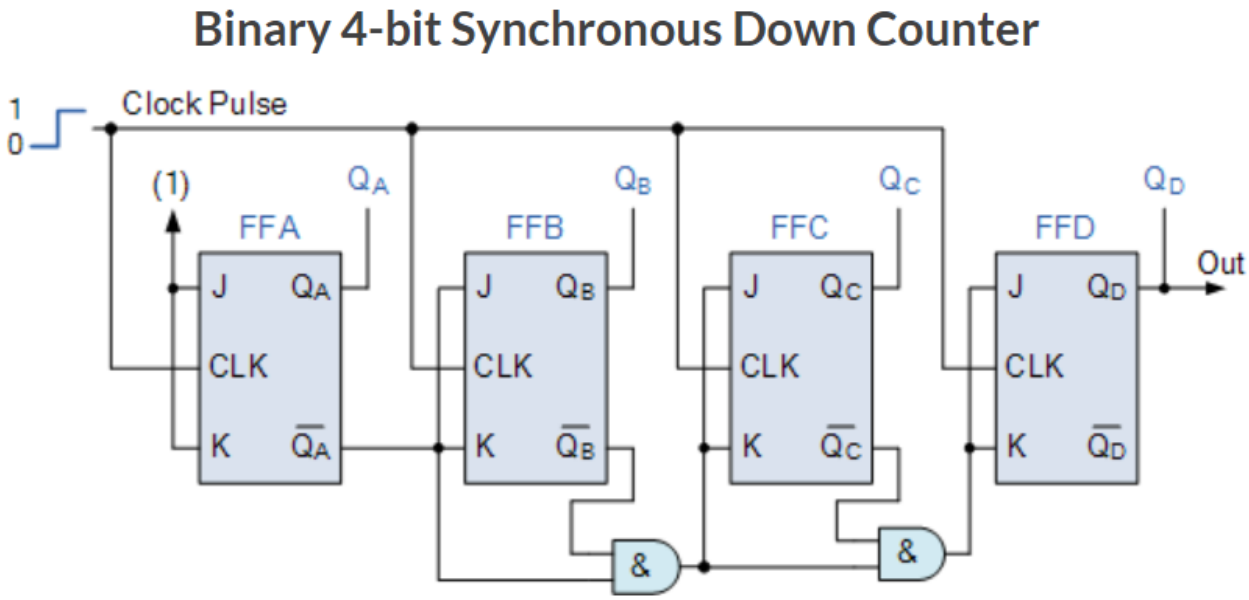
- If we enable each JK flip-flop to toggle based on whether or not all preceding flip-flop outputs (Q) are “HIGH” we can obtain the same counting sequence as with the asynchronous circuit but without the ripple effect, since each flip-flop in this circuit will be clocked at exactly the same time.
- Then as there is no inherent propagation delay in synchronous counters, because all the counter stages are triggered in parallel at the same time, the maximum operating frequency of this type of frequency counter is much higher than that for a similar asynchronous counter circuit.

4-bit Synchronous Counter Waveform Timing Diagram



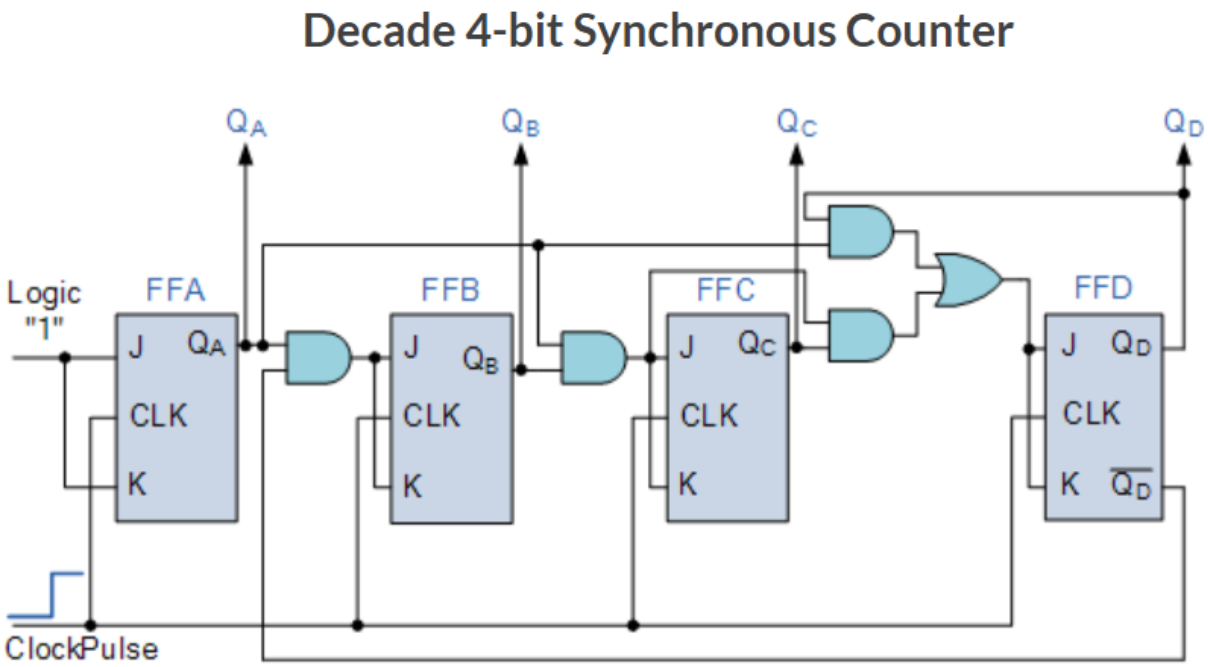
Synchronous Down Counter

- we can easily construct a **4-bit Synchronous Down Counter** by connecting the AND gates to the Q output of the flip-flops as shown to produce a waveform timing diagram the reverse of the above. Here the counter starts with all of its outputs HIGH (1111) and it counts down on the application of each clock pulse to zero, (0000) before repeating again.



Synchronous Decade Counter

- A 4-bit decade synchronous counter can also be built using synchronous binary counters to produce a count sequence from 0 to 9. A standard binary counter can be converted to a decade (decimal 10) counter with the aid of some additional logic to implement the desired state sequence. After reaching the count of "1001", the counter recycles back to "0000". We now have a decade or **Modulo-10** counter.



Synchronous Decade Counter

- The additional AND gates detect when the counting sequence reaches “1001”, (Binary 10) and causes flip-flop FF3 to toggle on the next clock pulse. Flip-flop FF0 toggles on every clock pulse. Thus, the count is reset and starts over again at “0000” producing a synchronous decade counter.

Exercise

- 1. Design a synchronous Mod-10 counter to count in the sequence 0,2,4,5,6,8
- 2. Design a Synchronous Mod-8 counter. A control input may be used that allow the counter to count in the up sequence or down sequence.

Reference

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Thankyou